ATSENSE-101/ATSENSE-201(H)/ATSENSE-301(H)

Multi-Channel Sigma-Delta Analog Front End

DATASHEET

Description

ATSENSE-101/ATSENSE-201(H)/ATSENSE-301(H) are multi-channel analog front end devices which integrate three, four or seven simultaneously sampled Sigma-Delta A/D converters, a high-precision voltage reference with up to 10 ppm/°C temperature stability (H-versions), a programmable current signal amplification, a temperature sensor and an SPI interface. When used in data acquisition and energy measurement applications in combination with the Atmel® ATSAM4C device family that features a dedicated Cortex®-M4 processor and metrology library and a variety of sensors including Shunt, CT and Rogowski coils, the ATSENSE-101/ATSENSE-201(H)/ATSENSE-301(H) exceeds ANSI C12.20-2002 and IEC 62053-22 metering accuracy classes of up to 0.2% over 3000:1 current range.

Features

- Analog Front End
  - Single-phase (ATSENSE-101), Dual-phase (ATSENSE-201(H)) or Poly-phase (ATSENSE-301(H)) Energy Metering Analog Front End Suitable for Atmel MCUs and Metrology Library
  - Compliant with Class 0.2 Standards (ANSI C12.20-2002 and IEC 62053-22)
  - Three, Four or Seven Sigma-Delta ADC Measurement Channels: One, Two or Three Voltages, Two or Four Currents, 102 dB Dynamic Range
  - Current Channels with Pre-Gain (x1, x2, x4, x8)
  - Supports Shunt, Current Transformer and Rogowski Coils
  - Dedicated Current Channel for Anti-tamper Measurement
  - Integrated SINC Decimation Filters. Output Data Rate: 16 kSps typical
  - Integrated 2.8V LDO Regulator to Supply Analog Functions
  - 3.0V to 3.6V Operation, Ultra Low Power: < 2.5 mW typical/Channel @ 3.3V
  - Specified for T_J = [-40°C; +100°C]
- Precision Voltage Reference
  - Standard 1.2V Output Voltage with Possible External Bypass
  - Temperature Drift: 50 ppm typical (ATSENSE-101/ATSENSE-201/ATSENSE-301)
  - Temperature Drift: 10 ppm typical (ATSENSE-201H/ATSENSE-301H)
  - Factory-measured Temperature Drift and Die Temperature Sensor to Perform Software Correction

- Digital Interface
  - 8 MHz Serial Peripheral Interface (SPI) Compatible Mode 1 (8-bit) for ADC Data and AFE Controls
  - Interrupt Output Line Signaling ADC End-of-Conversion, Underrun and Overrun
- Package
  - 32-lead TQFP, 7 x 7 x 1.4 mm
  - 20-lead SOIC, 12.8 x 7.5 x 2.3 mm

1. Block Diagrams

Figure 1-1. ATSENSE-301(H) Functional Block Diagram

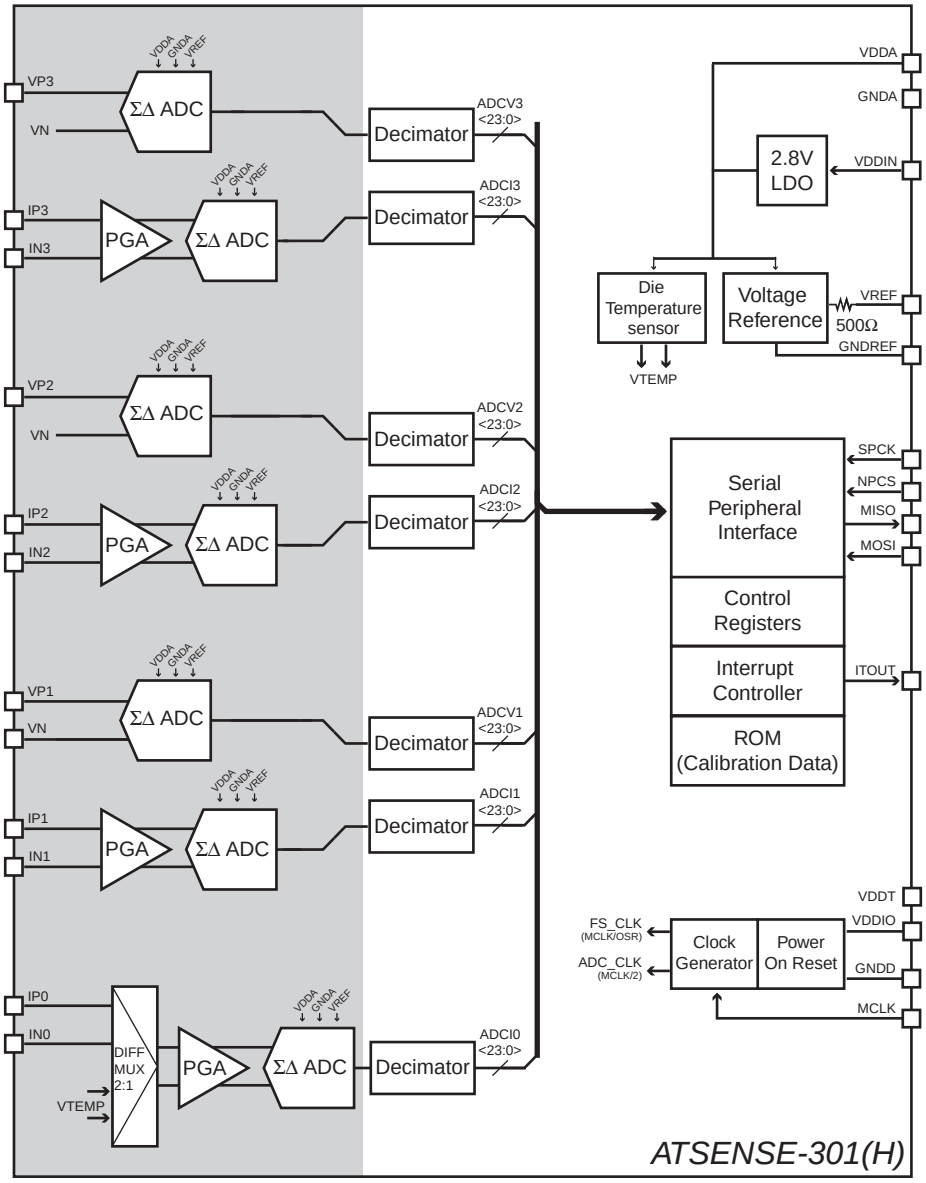


Figure 1-2. ATSENSE-201(H) Functional Block Diagram

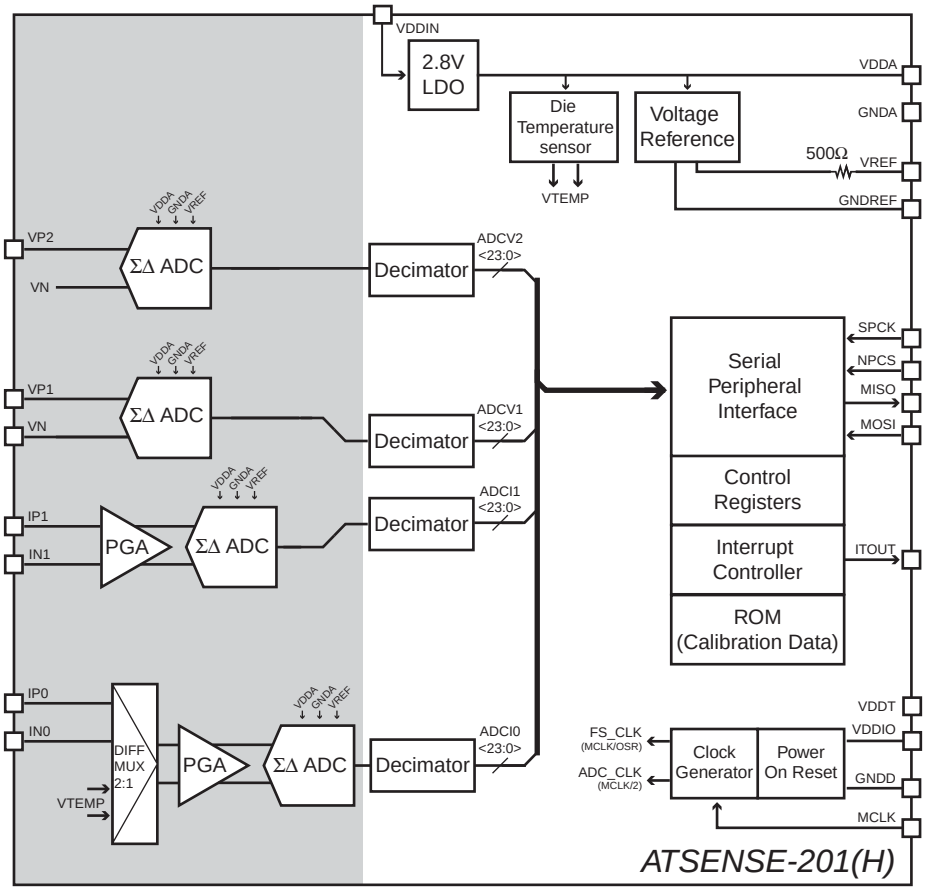
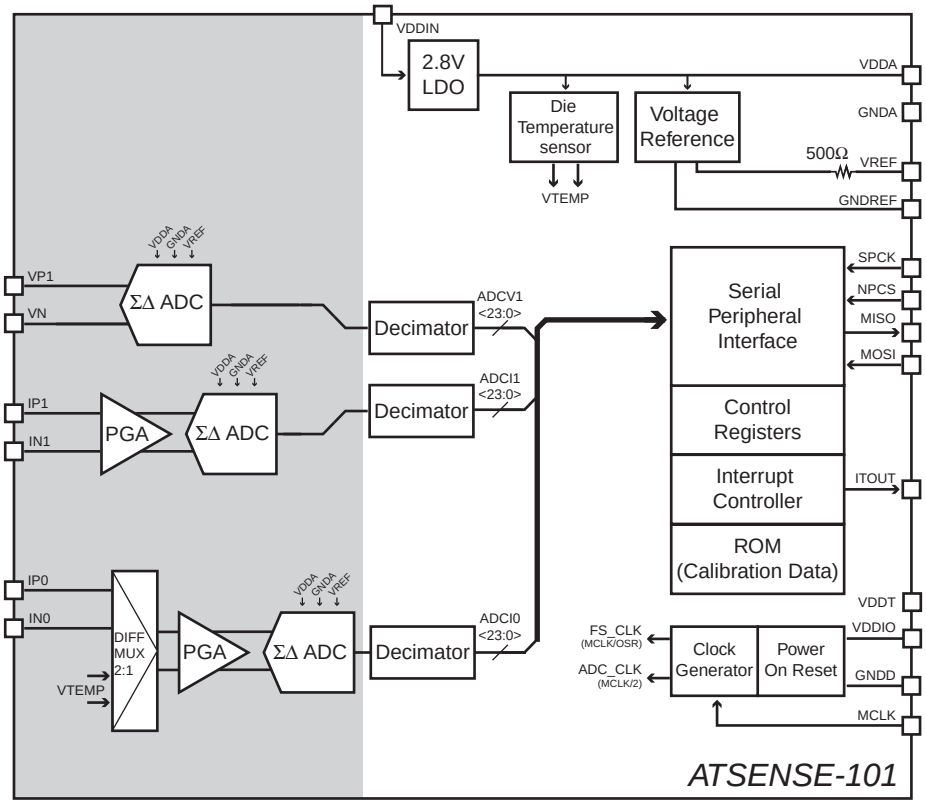


Figure 1-3. ATSENSE-101 Functional Block Diagram



2. Package and Pinout

2.1 ATSENSE-201(H) / ATSENSE-301(H)

Figure 2-1. 32-lead LQFP Package

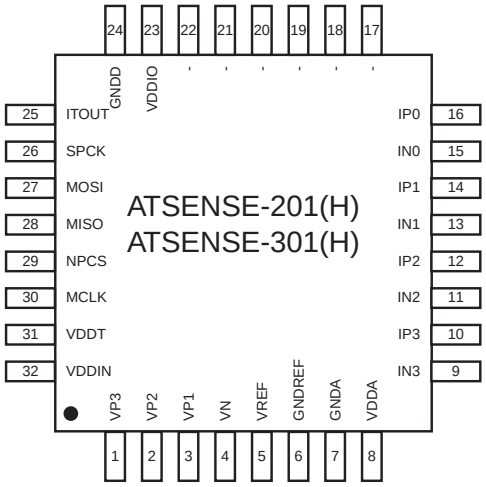


Table 2-1. ATSENSE-201(H) / ATSENSE-301(H) Pin Description

Pin Name	I/O	Pin Number	Type	Function
VP3[1]	Input	1	Analog	Voltage channel 3, positive input
VP2	Input	2	Analog	Voltage channel 2, positive input
VP1	Input	3	Analog	Voltage channel 1, positive input
VN	Input	4	Analog	Voltage channels negative input
VREF	In / Out	5	Analog	Voltage reference output and ADCs reference buffer input
GNDREF	Ground	6	Ground	Voltage reference ground pin
GNDA	Ground	7	Ground	Ground pin for low noise analog circuits and low noise negative ADC reference
VDDA	In / Out	8	Analog	2.8V LDO output and analog circuits power supply input
IN3[1]	Input	9	Analog	Current channel 3, negative input
IP3[1]	Input	10	Analog	Current channel 3, positive input
IN2[1]	Input	11	Analog	Current channel 2, negative input
IP2[1]	Input	12	Analog	Current channel 2, positive input
IN1	Input	13	Analog	Current channel 1, negative input
IP1	Input	14	Analog	Current channel 1, positive input
IN0	Input	15	Analog	Current channel 0 (Tamper), negative input
IP0	Input	16	Analog	Current channel 0 (Tamper), positive input
-	-	17 .. 22	-	Not connected. Connect to ground
VDDIO	Input	23	Power	Power supply input pin for digital I/O and digital core circuits
GNDD	Ground	24	Ground	Ground pin for digital I/O and digital core circuits

Table 2-1. ATSENSE-201(H) / ATSENSE-301(H) Pin Description (Continued)

Pin Name	I/O	Pin Number	Type	Function
ITOUT	Output	25	Digital	Interrupt output line. Open-drain
SPCK	Input	26	Digital	SPI port: serial clock
MOSI	Input	27	Digital	SPI port: master output slave input
MISO	Output	28	Digital	SPI port: master input slave output
NPCS	Input	29	Digital	SPI port: active-low chip select
MCLK	Input	30	Digital	Master clock input
VDDT	Input	31	Power	Pin reserved for test. Connect to VDDIN / VDDIO plane
VDDIN	Input	32	Power	2.8V LDO power supply input pin

Note: 1. Only in ATSENSE-301(H) devices. In ATSENSE-201(H) devices, these pins are not internally connected and Atmel recommends to connect them to ground.

2.2 ATSENSE-101

Figure 2-2. 20-lead SOIC Package

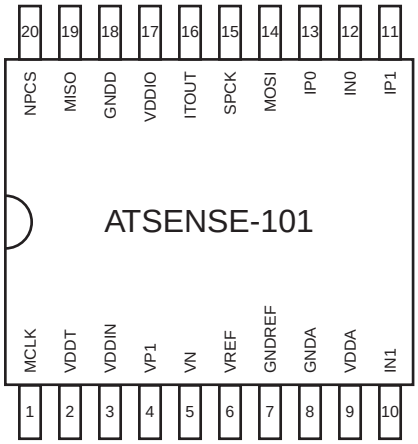
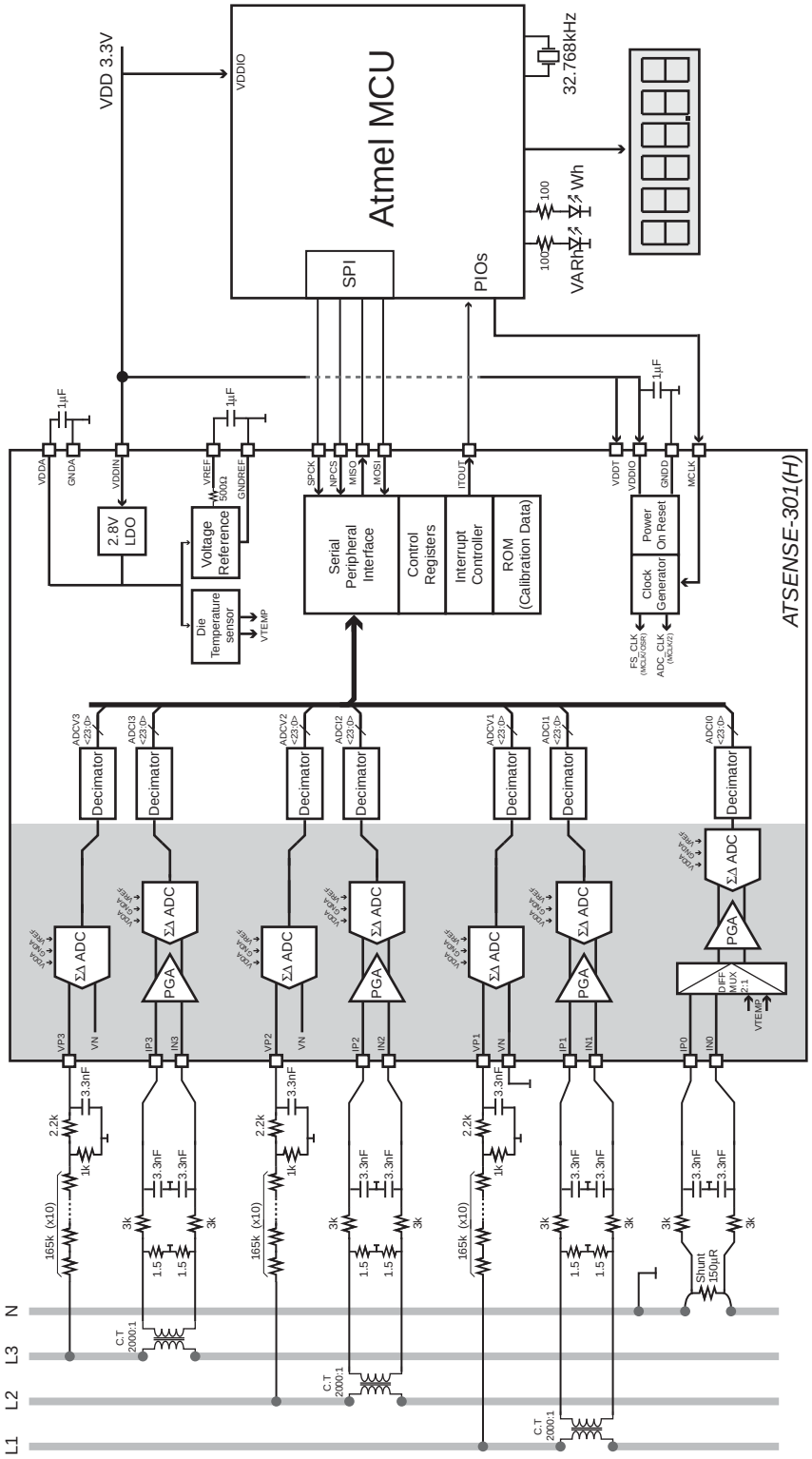


Table 2-2. ATSENSE-101 Pin Description

Pin Name	I/O	Pin Number	Type	Function
MCLK	Input	1	Digital	Master clock Input
VDDT	Input	2	Power	Pin reserved for test. Connect to VDDIN / VDDIO plane
VDDIN	Input	3	Power	2.8V LDO Power supply input pin
VP1	Input	4	Analog	Voltage channel 1, positive input
VN	Input	5	Analog	Voltage channel negative input
VREF	In / Out	6	Analog	Voltage reference output and ADCs reference buffer input
GNDREF	Ground	7	Ground	Voltage reference ground pin
GNDA	Ground	8	Ground	Ground pin for low noise analog circuits and low noise negative ADC reference
VDDA	In / Out	9	Analog	2.8V LDO output and analog circuits power supply input
IN1	Input	10	Analog	Current channel 1, negative input
IP1	Input	11	Analog	Current channel 1, positive input
IN0	Input	12	Analog	Current channel 0 (Tamper), negative input
IP0	Input	13	Analog	Current channel 0 (Tamper), positive input
MOSI	Input	14	Digital	SPI port: master output slave input
SPCK	Input	15	Digital	SPI port: serial clock
ITOUT	Output	16	Digital	Interrupt output line. open drain
VDDIO	Input	17	Power	Power supply input pin for digital I/O and digital core circuits
GNDD	Ground	18	Ground	Ground pin for digital I/O and digital core circuits
MISO	Output	19	Digital	SPI port: master input slave output
NPCS	Input	20	Digital	SPI port: active-low chip select

3. Application Block Diagram

Figure 3-1. ATSENSE-301(H) Typical Application Block Diagram



Typical 200A (Imax), 3-phase, 4-Wire Smart Meter based on Atmel Metrology Solution

Figure 3-2. ATSENSE-201(H) Typical Application Block Diagram

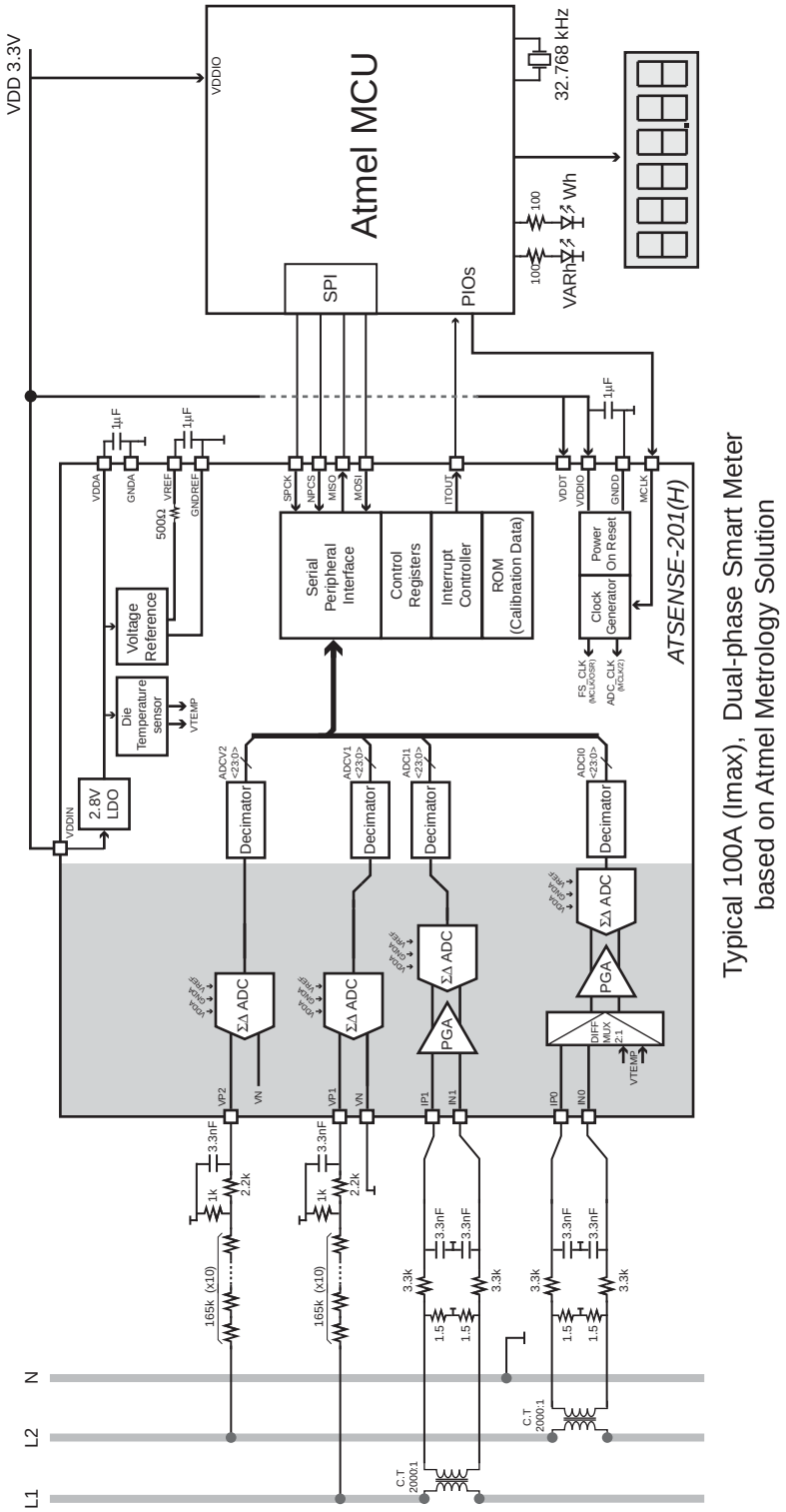
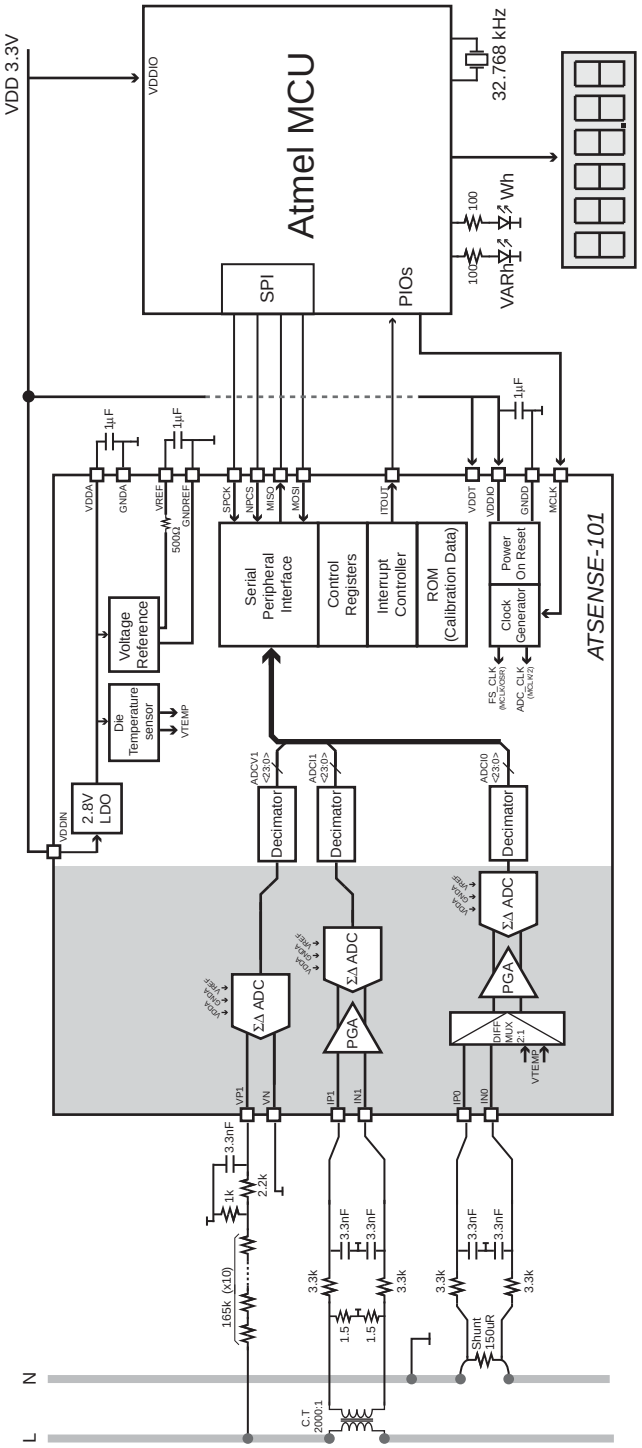


Figure 3-3. ATSENSE-101 Typical Application Block Diagram



Typical 100A (Imax), Single-phase with anti-tamper Smart Meter based on Atmel Metrology Solution

4. Functional Description

4.1 Conversion Channels

ATSENSE-101/ATSENSE-201(H)/ATSENSE-301(H) devices feature three types of acquisition channels:

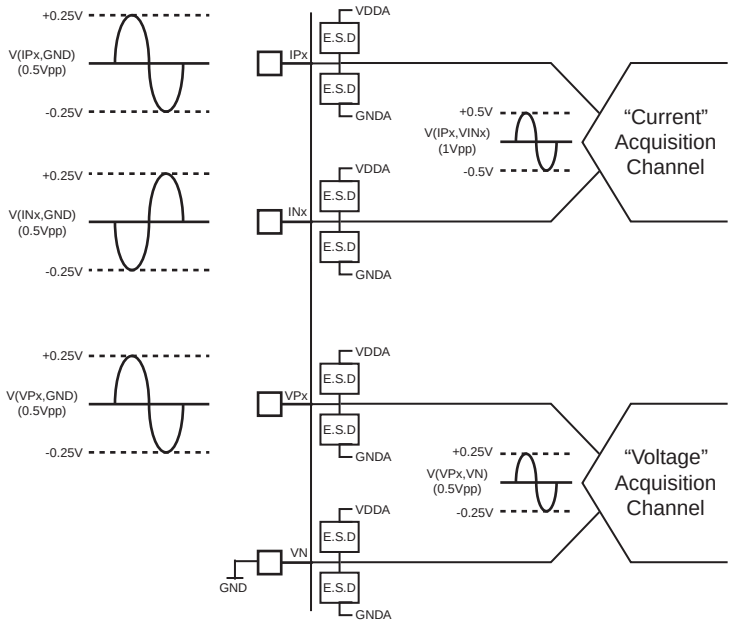
- Voltage channels
- Current channels
- Tamper and temperature channels

All these channels are built around the same Sigma-Delta A/D converter. The voltage reference of this converter is the VREF pin voltage referred to ground (GNDA pin). This reference voltage can be internally or externally sourced. The converter sampling rate is MCLK/4, typically 1.024 MHz. An external low-pass filter, typically a passive R-C network, is required at each ADC input to reject frequency images around this sampling frequency (anti-alias).

ATSENSE-101/ATSENSE-201(H)/ATSENSE-301(H) analog inputs are designed to sample 0V centered signals. As these inputs have internal ESD protection devices connected to GNDA, the maximum input signal level defined in the electrical characteristics, typically ±0.25V, must be respected to avoid leakage in these devices.

Refer to Figure 4-1, "Analog Inputs: Recommended Input Range".

Figure 4-1. Analog Inputs: Recommended Input Range



Voltage channels have single-ended inputs referred to the VN pin. The VN pin must be connected to a low noise ground. The user must take care that no voltage drop on the ground net is sampled by the ADC by non-optimum connection of the VN pin.

Current channels and the tamper channel have a programmable gain amplifier (PGA) to accommodate low input signals. The PGA improves the dynamic range of the channel as the input referred noise is reduced when gain increases. The PGA does not introduce any delay or bandwidth limitation on the current channels compared to the voltage channels. The channels (voltage or current) are always sampled synchronously. The input impedance of the PGA depends on the programmed gain.

The tamper channel features an input multiplexer to perform both the neutral current measurement and the die temperature measurement. The tamper channel has a PGA to accommodate low output level current sensors. Programmed gain can be changed when switching from the tamper to the die temperature sensor source.

4.2 Voltage Reference, Die Temperature Measurement and Calibration Registers

4.2.1 Voltage Reference

ATSENSE-101/ATSENSE-201(H)/ATSENSE-301(H) embed an analog voltage reference with a typical output voltage of 1.144V. The temperature drift of the voltage reference can be approximated by a linear fit. For H grade parts, the temperature drift is measured during manufacturing and stored in the calibration registers (ROM). Two measurements are made: one at a low temperature, TL, and another at a high temperature, TH. At both temperatures TL and TH, VREF voltage and ADC_TEMP_OUT (ADC I0 reading of the temperature sensor) parameters are saved. From the data obtained, the user can implement a software compensation of the voltage reference.

4.2.2 Die Temperature Sensor

To measure the internal die temperature, ATSENSE-101/ATSENSE-201(H)/ATSENSE-301(H) devices embed a dedicated analog die temperature sensor that is multiplexed on the tamper channel (ADC I0). By measuring the die temperature periodically and by using the calibration bits, channel gain drifts over temperature due to the voltage reference can be corrected.

To set the ADC to measure the temperature sensor, the user must set the TEMPMEAS bit in ADC I0 control register and ensure that the channel gain is set to x1 (0dB).

Once the temperature measurement is selected, the ADC starts to output samples corresponding to the temperature sensor. The first four samples account for internal digital filters settling and must be ignored. Then, in order to have a repeatable temperature acquisition, the user must average the ADC output over a minimum of 64 samples. By following this procedure, the temperature acquisition set measurement exhibits a standard deviation of less than 0.25°C in repeatability.

To calculate the real die temperature from the ADC acquisition, the following formula applies:

$$T_J(°C) = ((ADC\_TEMP\_OUT / 2^{24}) \times 1.144 - 0.110) / 0.00049$$

where ADC_TEMP_OUT is the 24-bit output of ADC I0, averaged over 64 samples. Example: If ADC_TEMP_OUT = 1777345, the corresponding die temperature is T_J = 22.8°C.

Because the temperature sensor is not offset-calibrated, the absolute temperature reading exhibits a large deviation (typically ±15°C).

4.2.3 Calibration Registers

The registers used in the voltage reference compensation are listed in Table 4-1. The four parameters stored, VREF and ADC_TEMP_OUT at TL and TH, are:

- REF_TL[11:0] and REF_TH[11:0]
- TEMP_TL[11:0] and TEMP_TH[11:0]

The following rule applies to recover the real values of VREF from the 12-bit coded values in the product registers:

- VREF(TL) = 1.120V + REF_TL[11:0] * 25µV
- VREF(TH) = 1.120V + REF_TH[11:0] * 25µV

Note: REF_TL[11:0] and REF_TH[11:0] are unsigned 12-bit integers.

The following rule applies to recover the real values of ADC_TEMP_OUT from the 12-bit coded values in the product registers:

- ADC_TEMP_OUT[23:0](TL) = TEMP_TL[11:0] << 12
- ADC_TEMP_OUT[23:0](TH) = TEMP_TH[11:0] << 12

Note: TEMP_TL[11:0] and TEMP_TH[11:0] are signed 12-bit integers.

Table 4-1. Calibration Register Mapping

Offset	Register	Name	Access	Reset
0x41	Voltage Reference Value at TL: MSB	REF_TL_11_8	Read-only	0x-0
0x42	Voltage Reference Value at TL: LSB	REF_TL_7_0	Read-only	0x00
0x43	Temperature Sensor Value (read by ADC) at TL: MSB	TEMP_TL_11_8	Read-only	0x-0
0x44	Temperature Sensor Value (read by ADC) at TL: LSB	TEMP_TL_7_0	Read-only	0x00
0x45	Voltage Reference Value at TH: MSB	REF_TH_11_8	Read-only	0x-0
0x46	Voltage Reference Value at TH: LSB	REF_TH_7_0	Read-only	0x00
0x47	Temperature Sensor Value (read by ADC) at TH: MSB	TEMP_TH_11_8	Read-only	0x-0
0x48	Temperature Sensor Value (read by ADC) at TH: LSB	TEMP_TH_7_0	Read-only	0x00

4.3 Voltage Reference Value at TL: MSB

Name: REF_TL_11_8

Access: Read-only

7	6	5	4	3	2	1	0
—	—	—	—	REF_TL[11:8]			

- **REF_TL[11:8]: 4 MSB of REF_TL[11:0]**

4.4 Voltage Reference Value at TL: LSB

Name: REF_TL_7_0

Access: Read-only

7	6	5	4	3	2	1	0
REF_TL[7:0]							

- **REF_TL[7:0]: 8 LSB of REF_TL[11:0]**

4.5 Temperature Sensor Value at TL: MSB

Name: TEMP_TL_11_8

Access: Read-only

7	6	5	4	3	2	1	0
—	—	—	—	TEMP_TL[11:8]			

- **TEMP_TL[11:8]: 4 MSB of TEMP_TL[11:0]**

4.6 Temperature Sensor Value at TL: LSB

Name: TEMP_TL_7_0

Access: Read-only

7	6	5	4	3	2	1	0
TEMP_TL[7:0]							

- **TEMP_TL[7:0]: 8 LSB of TEMP_TL[11:0]**

4.7 Voltage Reference Value at TH: MSB

Name: REF_TH_11_8

Access: Read-only

7	6	5	4	3	2	1	0
—	—	—	—	REF_TH[11:8]			

- **REF_TH[11:8]: 4 MSB of REF_TH[11:0]**

4.8 Voltage Reference Value at TH: LSB

Name: REF_TH_7_0

Access: Read-only

7	6	5	4	3	2	1	0
REF_TH[7:0]							

- **REF_TH[7:0]: 8 LSB of REF_TH[11:0]**

4.9 Temperature Sensor Value at TH: MSB

Name: TEMP_TH_11_8

Access: Read-only

7	6	5	4	3	2	1	0
—	—	—	—	TEMP_TH[11:8]			

- **TEMP_TH[11:8]: 4 MSB of TEMP_TH[11:0]**

4.10 Temperature Sensor Value at TH: LSB

Name: TEMP_TH_7_0

Access: Read-only

7	6	5	4	3	2	1	0
TEMP_TH[7:0]							

- **TEMP_TH[7:0]: 8 LSB of TEMP_TH[11:0]**

4.11 Correction Algorithm

For H-grade products, it is possible to compensate the drift of the voltage reference by using the calibration registers described above. The following formula is used to estimate VREF at a given temperature:

$$VREF(ADC\_TEMP\_OUT) = VREF(TL) + \frac{(ADC\_TEMP\_OUT\text{-}TEMP\_TL)}{(TEMP\_TH\text{-}TEMP\_TL)} \cdot (VREF(TH) - VREF(TL))$$

where:

- VREF(ADC_TEMP_OUT): Estimated VREF value when the temperature sensor reading is ADC_TEMP_OUT
- VREF(TL): VREF value at temperature TL retrieved from REF_TL[11:0]
- VREF(TH): VREF value at temperature TH retrieved from REF_TH[11:0]
- TEMP(TL): ADC_TEMP_OUT value at temperature TL retrieved from TEMP_TL[11:0]
- TEMP(TH): ADC_TEMP_OUT value at temperature TH retrieved from TEMP_TL[11:0]

5. SPI Controller

5.1 Description

The SPI controller is an interface between

- the serial peripheral interface communication port
- the decimation filter output data in 2’s complement format
- the analog functions (ADC, LDO and reference voltage)

The SPI port provides read/write access to internal registers (Table 4-1 on page 14). This serial port features a burst transmission mode with variable data size that captures up to 7 x 32-bit ADC output results into one single access.

5.2 SPI Serial Port

5.2.1 Description

The SPI interface protocol permits writing to and/or reading registers. Moreover, a burst mode allows the fast acquisition of multiple registers or a write on multiple registers. With this function, the size of the data can easily vary. For example, two adjacent registers can be accessed at the same time by addressing the first register (lowest address value) and extending the quantity of serial clock edges.

The SPI interface is compatible with SPI modes 1 and 2. Data are latched on falling edges of SCLK while they are generated on the rising edges of SCLK. The idle state of SCLK can be either high or low.

5.2.2 Protocol

A transfer occurs when the NPCS signal is low. The incoming stream on MOSI is decoded on SCLK falling edge.

The first received bit indicates the direction of the operation, where 0 indicates a write and 1 a read.

The seven subsequent bits contain the address of the register to read or write.

The following bytes are data which are either emitted on the MISO line in case of a read operation, or decoded on the MOSI line in case of a write operation.

The first data address corresponds to the first decoded address. The address pointer is then incremented each time a new byte is read or written.

The operation ends when NPCS goes high.

If NPCS goes high before the end of a byte transfer, the current byte operation is cancelled. For a read operation, no further data are sent on the MISO line. For a write operation, no data is written into the currently decoded address. All previous byte operations are valid.

Figure 5-1. MODE 1 Multi-Byte Write Operation

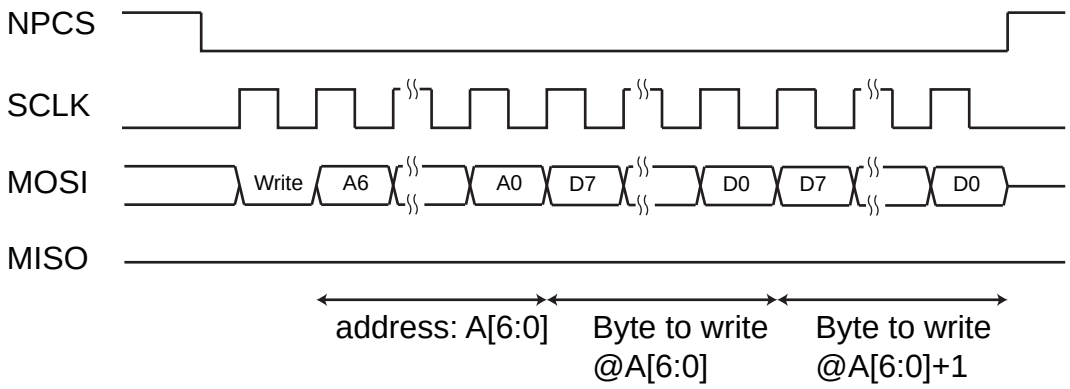


Figure 5-2. MODE 2 Multi-Byte Write Operation

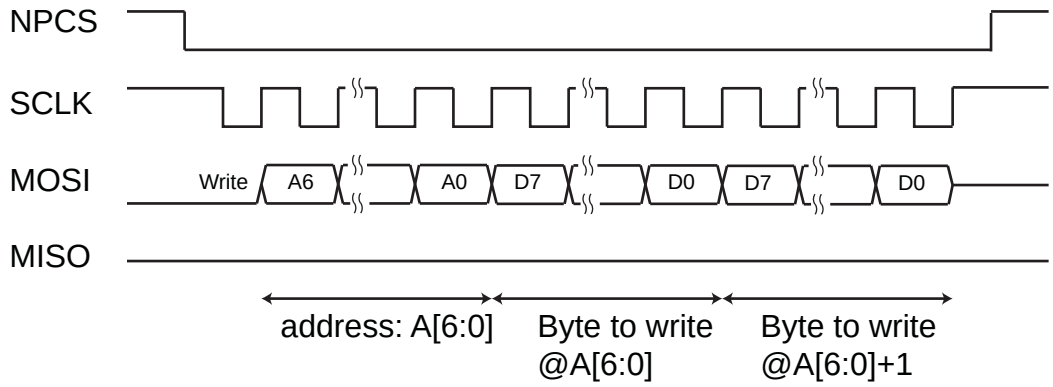


Figure 5-3. MODE 1 Multi-Byte Read Operation

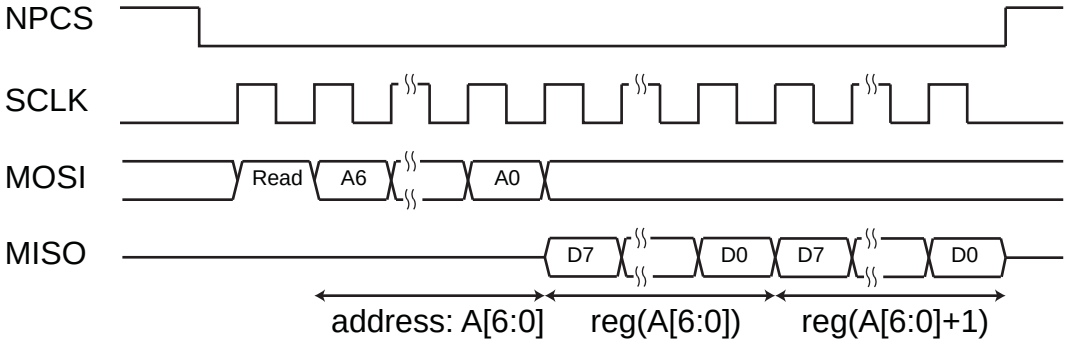
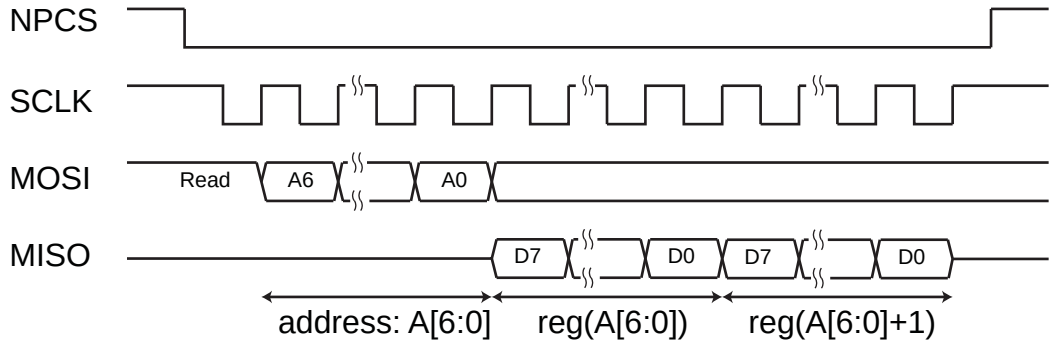


Figure 5-4. MODE 2 Multi-Byte Read Operation



6. Interrupt Controller

The Interrupt Controller generates three interrupts:

- ADC ready interrupt
- Overrun interrupt
- Underrun interrupt

The interrupts can be detected by either polling the Interrupt Status register (ITSR) and/or by configuring the ITOUT output line. Because it is open-drain, this output needs to be pulled-up to VDDIO.

When activated, the ITOUT line goes low when an interrupt event occurs. It goes into Hi-Z state as soon as the interrupt source has been reset.

Refer to “Output Interrupt Line Control Register” on page 43, “Interrupt Control Register” on page 44 and “Interrupt Status Register” on page 45 for more information on the interrupt line configuration

6.1 ADC Ready

The ADC_RDY interrupt rises at each new conversion frame, thus when an ADC is enabled, it reports that a new set of data is available.

It is reset either on the read of at least one ADC register (addresses from ADCI0_TAG to ADCV3_7_0) or on the read of the status register.

As the user may not need all converted values of the ADCs, only the first access to an ADC data is taken into account to reset this interrupt.

6.2 Overrun

If ADC data acquisition registers are accessed twice within the same conversion period, the OVRES interrupt rises.

It is reset on the read of the status register.

6.3 Underrun

If two synchronous signals occur without any ADC data acquisition, the UNDES interrupt rises.

It is reset on the read of the status register.

7. SPI Controller User Interface

Table 7-1. Register Mapping

Offset	Register	Name	Access	Reset
0x00[2]	ADCI0 TAG Register	ADCI0_TAG	Read-only	0x01
0x01 (0x00[1])	ADCI0 Output Bits 23 to 16 Read Register	ADCI0_23_16	Read-only	0x00
0x02 (0x01[1])	ADCI0 Output Bits 15 to 8 Read Register	ADCI0_15_8	Read-only	0x00
0x03[2]	ADCI0 Output Bits 7 to 0 Read Register	ADCI0_7_0	Read-only	0x00
0x04[2]	ADCI1 TAG Register	ADCI1_TAG	Read-only	0x02
0x05 (0x02[1])	ADCI1 Output Bits 23 to 16 Read Register	ADCI1_23_16	Read-only	0x00
0x06 (0x03[1])	ADCI1 Output Bits 15 to 8 Read Register	ADCI1_15_8	Read-only	0x00
0x07[2]	ADCI1 Output Bits 7 to 0 Read Register	ADCI1_7_0	Read-only	0x00
0x08[2]	ADCV1_TAG Register	ADCV1_TAG	Read-only	0x03
0x09 (0x04[1])	ADCV1 Output Bits 23 to 16 Read Register	ADCV1_23_16	Read-only	0x00
0x0a (0x05[1])	ADCV1 Output Bits 15 to 8 Read Register	ADCV1_15_8	Read-only	0x00
0x0b[2]	ADCV Output Bits 7 to 0 Register	ADCV1_7_0	Read-only	0x00
0x0c[2]	ADCI2_TAG Register[3]	ADCI2_TAG	Read-only	0x04
0x0d (0x06[1])	ADCI2 Output Bits 23 to 16 Read Register[3]	ADCI2_23_16	Read-only	0x00
0x0e (0x07[1])	ADCI2 Output Bits 15 to 8 Read Register[3]	ADCI2_15_8	Read-only	0x00
0x0f[2]	ADCI2 Output Bits 7 to 0 Read Register[3]	ADCI2_7_0	Read-only	0x00
0x10[2]	ADCV2_TAG Register[3]	ADCV2_TAG	Read-only	0x05
0x11 (0x08[1])	ADCV2 Output Bits 23 to 16 Read Register[3]	ADCV2_23_16	Read-only	0x00
0x12 (0x09[1])	ADCV2 Output Bits 15 to 8 Read Register[3]	ADCV2_15_8	Read-only	0x00
0x13[2]	ADCV2 Output Bits 7 to 0 Read Register[3]	ADCV2_7_0	Read-only	0x00
0x14[2]	ADCI3_TAG Register[3]	ADCI3_TAG	Read-only	0x06
0x15 (0x0a[1])	ADCI3 Output Bits 23 to 16 Read Register[3]	ADCI3_23_16	Read-only	0x00
0x16 (0x0b[1])	ADCI3 Output Bits 15 to 8 Read Register[3]	ADCI3_15_8	Read-only	0x00
0x17[2]	ADCI3 Output Bits 7 to 0 Read Register[3]	ADCI3_7_0	Read-only	0x00
0x18[2]	ADCV3_TAG Register[3]	ADCV3_TAG	Read-only	0x07
0x19 (0x0c[1])	ADCV3 Output Bits 23 to 16 Read Register[3]	ADCV3_23_16	Read-only	0x00
0x1a (0x0d[1])	ADCV3 Output Bits 15 to 8 Read Register[3]	ADCV3_15_8	Read-only	0x00
0x1b[2]	ADCV3 Output Bits 7 to 0 Read Register[3]	ADCV3_7_0	Read-only	0x00
0x20	ADCI0 Controls Register	SDI0	Read/Write	0x00
0x21	ADCI1 Controls Register	SDI1	Read/Write	0x00
0x22	ADCV1 Controls Register	SDV1	Read/Write	0x00
0x23	ADCI2 Controls Register[3]	SDI2	Read/Write	0x00
0x24	ADCV2 Controls Register[3]	SDV2	Read/Write	0x00
0x25	ADCI3 Controls Register[3]	SDI3	Read/Write	0x00
0x26	ADCV3 Controls Register[3]	SDV3	Read/Write	0x00

Table 7-1. Register Mapping

Offset	Register	Name	Access	Reset
0x27	Analog Controls Register	ANA_CTRL	Read/Write	0x00
0x28	ATSENSE Configuration Register	ATCFG	Read/Write	0x03
0x29	ATSENSE Status Register	ATSR	Read-only	—
0x2a	Output Interrupt Line Control Register	ITOUTCR	Read/Write	0x04
0x2b	Interrupt Control Register	ITCR	Read/Write	0x00
0x2c	Interrupt Status Register	ITSR	Read-only	0x00
0x2d	Software Reset Register	SOFT_NRESET	Write-only	0x00

Notes:
1. Address value if the MSB mode is activated (see Section 7.37 ”ATSENSE Configuration Register”).
2. This register cannot be read if the MSB mode is activated (see Section 7.37 ”ATSENSE Configuration Register”).
3. Only for ATSENSE-201(H)/ATSENSE-301(H).

7.1 ADCI0 TAG Register

Name: ADCI0_TAG

Access: Read-only

7	6	5	4	3	2	1	0
–	–	DATA_VALID	TEMPMEAS	TAGI0			

- **TAGI0: TAG of the Anti-tamper ADC Channel**

TAGI0 is equal to 1.

- **TEMPMEAS: Temperature Measurement Status**

0: The external input of the TAMPER ADC is measured.

1: The temperature sensor input of the TAMPER ADC is measured.

- **DATA_VALID: I0 Channel Data Validity Status**

0: The current data is not valid.

1: The current data is valid.

When the source of the ADCI0 channel switches, the decimation filter needs a few samples to stabilize its response (group delay of the filter). Data acquired while DATA_VALID is null are not valid.

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.2 ADCI0 Output Bits 23 to 16 Read Register

Name: ADCI0_23_16

Access: Read-only

7	6	5	4	3	2	1	0
ADCI0[23:16]							

- **ADCI0_23_16: Bits 23 to 16 of the Anti-tamper ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.3 ADCI0 Output Bits 15 to 8 Read Register

Name: ADCI0_15_8

Access: Read-only

7	6	5	4	3	2	1	0
ADCI0[15:8]							

- **ADCI0_15_8: Bits 15 to 8 of the Anti-tamper ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.4 ADCI0 Output Bits 7 to 0 Read Register

Name: ADCI0_7_0

Access: Read-only

7	6	5	4	3	2	1	0
ADCI0[7:0]							

- **ADCI0_7_0: Bits 7 to 0 of the Anti-tamper ADC Channel**

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.5 ADCI1 TAG Register

Name: ADCI1_TAG

Access: Read-only

7	6	5	4	3	2	1	0
TAGI1							

- **TAGI1: TAG of the I1 ADC Channel**

TAGI1 is equal to 2.

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.6 ADCI1 Output Bits 23 to 16 Read Register

Name: ADCI1_23_16

Access: Read-only

7	6	5	4	3	2	1	0
ADCI1[23:16]							

- **ADCI1_23_16: Bits 23 to 16 of the I1 ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.7 ADCI1 Output Bits 15 to 8 Read Register

Name: ADCI1_15_8

Access: Read-only

7	6	5	4	3	2	1	0
ADCI1[15:8]							

- **ADCI1_15_8: Bits 15 to 8 of the I1 ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.8 ADCI1 Output Bits 7 to 0 Read Register

Name: ADCI1_7_0

Access: Read-only

7	6	5	4	3	2	1	0
ADCI1[7:0]							

- **ADCI1_7_0: bits 7 to 0 of the I1 ADC channel**

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.9 ADCV1 TAG Register

Name: ADCV1_TAG

Access: Read-only

7	6	5	4	3	2	1	0
TAGV1							

- **TAGV1: TAG of the V1 ADC Channel**

TAGV1 is equal to 3.

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.10 ADCV1 Output Bits 23 to 16 Read Register

Name: ADCV1_23_16

Access: Read-only

7	6	5	4	3	2	1	0
ADCV1[23:16]							

- **ADCV1_23_16: Bits 23 to 16 of the V1 ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.11 ADCV1 Output Bits 15 to 8 Read Register

Name: ADCV1_15_8

Access: Read-only

7	6	5	4	3	2	1	0
ADCV1[15:8]							

- **ADCV1_15_8: Bits 15 to 8 of the V1 ADC Channel**

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.12 ADCV1 Output Bits 7 to 0 Read Register

Name: ADCV1_7_0

Access: Read-only

7	6	5	4	3	2	1	0
ADCV1[7:0]							

- **ADCV1_7_0: Bits 7 to 0 of the V1 ADC Channel**

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.13 ADCI2 TAG Register

Name: ADCI2_TAG

Access: Read-only

7	6	5	4	3	2	1	0
TAGI2							

- **TAGI2: TAG of the I2 ADC Channel**

TAGI2 is equal to 4.

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.14 ADCI2 Output Bits 23 to 16 Read Register

Name: ADCI2_23_16

Access: Read-only

7	6	5	4	3	2	1	0
ADCI2[23:16]							

- **ADCI2_23_16: Bits 23 to 16 of the I2 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.15 ADCI2 Output Bits 15 to 8 Read Register

Name: ADCI2_15_8

Access: Read-only

7	6	5	4	3	2	1	0
ADCI2[15:8]							

- **ADCI2_15_8: Bits 15 to 8 of the I2 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.16 ADCI2 Output Bits 7 to 0 Read Register

Name: ADCI2_7_0

Access: Read-only

7	6	5	4	3	2	1	0
ADCI2[7:0]							

- **ADCI2_7_0: Bits 7 to 0 of the I2 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.17 ADCV2 TAG Register

Name: ADCV2_TAG

Access: Read-only

7	6	5	4	3	2	1	0
TAGV2							

- **TAGV2: TAG of the V2 ADC Channel**

TAGV2 is equal to 5.

This register is available only in ATSENSE-201(H)/ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.18 ADCV2 Output Bits 23 to 16 Read Register

Name: ADCV2_23_16

Access: Read-only

7	6	5	4	3	2	1	0
ADCV2[23:16]							

- **ADCV2_23_16: Bits 23 to 16 of the V2 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.19 ADCV2 Output Bits 15 to 8 Read Register

Name: ADCV2_15_8

Access: Read-only

7	6	5	4	3	2	1	0
ADCV2[15:8]							

- **ADCV2_15_8: Bits 15 to 8 of the V2 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H).

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.20 ADCV2 Output Bits 7 to 0 Read Register

Name: ADCV2_7_0

Access: Read-only

7	6	5	4	3	2	1	0
ADCV2[7:0]							

- **ADCV2_7_0: Bits 7 to 0 of the V2 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H).

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.21 ADCI3 TAG Register

Name: ADCI3_TAG

Access: Read-only

7	6	5	4	3	2	1	0
TAGI3							

- **TAGI3: TAG of the I3 ADC Channel**

TAGI3 is equal to 6.

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.22 ADCI3 Output Bits 23 to 16 Read Register

Name: ADCI3_23_16

Access: Read-only

7	6	5	4	3	2	1	0
ADCI3[23:16]							

- **ADCI3_23_16: Bits 23 to 16 of the I3 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.23 ADCI3 Output Bits 15 to 8 Read Register

Name: ADCI3_15_8

Access: Read-only

7	6	5	4	3	2	1	0
ADCI3[15:8]							

- **ADCI3_15_8: Bits 15 to 8 of the I3 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.24 ADCI3 Output Bits 7 to 0 Read Register

Name: ADCI3_7_0

Access: Read-only

7	6	5	4	3	2	1	0
ADCI3[7:0]							

- **ADCI3_7_0: Bits 7 to 0 of the I3 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.25 ADCV3 TAG Register

Name: ADCV3_TAG

Access: Read-only

7	6	5	4	3	2	1	0
TAGV3							

- **TAGV3: TAG of the V3 ADC Channel**

TAGV3 is equal to 7.

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.26 ADCV3 Output Bits 23 to 16 Read Register

Name: ADCV3_23_16

Access: Read-only

7	6	5	4	3	2	1	0
ADCV3[23:16]							

- **ADCV3_23_16: Bits 23 to 16 of the V3 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.27 ADCV3 Output Bits 15 to 8 Read Register

Name: ADCV3_15_8

Access: Read-only

7	6	5	4	3	2	1	0
ADCV3[15:8]							

- **ADCV3_15_8: Bits 15 to 8 of the V3 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

The address value of this register depends on the value of the MSB_MODE bit (see Table 7-1 on page 23).

7.28 ADCV3 Output Bits 7 to 0 Read Register

Name: ADCV3_7_0

Access: Read-only

7	6	5	4	3	2	1	0
ADCV3[7:0]							

- **ADCV3_7_0: Bits 7 to 0 of the V3 ADC Channel**

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

This register is not accessible if the MSB_MODE bit is enabled (see Section 7.37 on page 41).

7.29 ADCI0 Controls Register

Name: SDI0

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	GAIN		–	–	TEMPMEAS	ONADC

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 µs.

- **TEMPMEAS: Temperature Measurement Activation**

0: The external input of the TAMPER ADC is measured.

1: The temperature sensor input of the TAMPER ADC is measured.

This register must not be modified as long as the DATA_VALID bit is low (see “ADCI0 TAG Register” on page 25).

- **GAIN: Gain Configuration of the ADC**

Value	Name	Description
0	ADC_GAINX1	Input stage of the ADC has a gain of 1
1	ADC_GAINX2	Input stage of the ADC has a gain of 2
2	ADC_GAINX4	Input stage of the ADC has a gain of 4
3	ADC_GAINX8	Input stage of the ADC has a gain of 8

7.30 ADCI1 Controls Register

Name: SDI1

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	GAIN		–	–	–	ONADC

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 µs.

- **GAIN: Gain Configuration of the ADC**

Value	Name	Description
0	ADC_GAINX1	Input stage of the ADC has a gain of 1
1	ADC_GAINX2	Input stage of the ADC has a gain of 2
2	ADC_GAINX4	Input stage of the ADC has a gain of 4
3	ADC_GAINX8	Input stage of the ADC has a gain of 8

7.31 ADCV1 Controls Register

Name: SDV1

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ONADC

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 µs.

7.32 ADCI2 Controls Register

Name: SDI2

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	GAIN		–	–	–	ONADC

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 µs.

- **GAIN: Gain Configuration of the ADC**

Value	Name	Description
0	ADC_GAINX1	Input stage of the ADC has a gain of 1
1	ADC_GAINX2	Input stage of the ADC has a gain of 2
2	ADC_GAINX4	Input stage of the ADC has a gain of 4
3	ADC_GAINX8	Input stage of the ADC has a gain of 8

7.33 ADCV2 Controls Register

Name: SDV2

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ONADC

This register is available only in ATSENSE-201(H)/ATSENSE-301(H).

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 µs.

7.34 ADCI3 Controls Register

Name: SDI3

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	GAIN		–	–	–	ONADC

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 µs.

- **GAIN: Gain Configuration of the ADC**

Value	Name	Description
0	ADC_GAINX1	Input stage of the ADC has a gain of 1
1	ADC_GAINX2	Input stage of the ADC has a gain of 2
2	ADC_GAINX4	Input stage of the ADC has a gain of 4
3	ADC_GAINX8	Input stage of the ADC has a gain of 8

7.35 ADCV3 Controls Register

Name: SDV3

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ONADC

This register is available only in ATSENSE-201(H)/ATSENSE-301(H). In ATSENSE-201(H), it should be ignored.

- **ONADC: ADC Enable**

0: ADC is disabled.

1: ADC is enabled.

When set, this bit can be read at one only after 768 µs.

7.36 Analog Controls Register

Name: ANA_CTRL

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	ONLDO	ONREF	ONBIAS

- **ONBIAS: Enable of the Current Bias Generator**

0: The current bias generator is disabled.

1: The current bias generator is enabled.

- **ONREF: Enable of the Voltage Reference**

0: The voltage reference is disabled.

1: The voltage reference is enabled.

When set, this bit can be read at one after 768 µs.

- **ONLDO: Enable of the Internal LDO**

0: The LDO is disabled.

1: The LDO is enabled.

When set, this bit can be read at one after 928 µs.

7.37 ATSENSE Configuration Register

Name: ATCFG

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	MSB_MODE	–	–	OSR	

- **OSR: OSR of the Decimation Filters**

Value	Name	Description
0	OSR8	OSR of the system is 8
1	OSR16	OSR of the system is 16
2	OSR32	OSR of the system is 32
3	OSR64	OSR of the system is 64

The oversampling ratio (OSR) is the ratio between the input sampling rate F_{Sin}(ADC sampling rate, typically 1.024 MHz) and the output sampling rate F_{Sout} of the decimation filter. .

$$F_{Sout} = \frac{F_{Sin}}{OSR}$$

The OSR must be set before switching on any ADC. Its value must not be changed if any of the ADCs are operating.

- **MSB_MODE: Selection Between 32-bit or 16-bit ADC Mode**

Value	Name	Description
0	32BITS_MODE	The interface sends an 8-bit tag followed by the 24 bits of the ADC conversion (ADCx_TAG, ADCx_23_16, ADCx_15_8 and ADCx_7_0 registers).
1	16BITS_MODE	The interface sends the 16 MSB of the ADC conversion (ADCx_23_16 and ADCx_15_8 registers). The addresses of these registers are modified while ADCx_TAG and ADCx_7_0 are no longer readable.

7.38 ATSENSE Status Register

Name: ATSR

Access: Read-only

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	SYSRDY

- **SYSRDY: System Ready**

0: The system is not ready.

1: The system is ready.

Each time a soft or a hard reset is performed, the system operates initialization operations. ATSR indicates the end of these operations.

While ATSR is not high, no write access is possible in the registers.

7.39 Output Interrupt Line Control Register

Name: ITOUTCR

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	ADC_RDY_OUT	UNDES_OUT	OVRES_OUT

- **OVRES_OUT: Overrun Output Enable**

1: The OVRES interrupt activates the ITOUT output.

0: The OVRES interrupt does not activate the ITOUT output.

- **UNDES_OUT: Underrun Output Enable**

1: The UNDES interrupt activates the ITOUT output.

0: The UNDES interrupt does not activate the ITOUT output.

- **ADC_RDY_OUT: ADC Ready Output Enable**

1: The ADC_RDY interrupt activates the ITOUT output.

0: The ADC_RDY interrupt does not activate the ITOUT output.

7.40 Interrupt Control Register

Name: ITCR

Access: Read/Write

7	6	5	4	3	2	1	0
–	–	–	–	–	ADC_RDY_EN	UNDES_EN	OVRES_EN

- **OVRES_EN: Overrun Interrupt Enable**

0: The generation of the overrun interrupt is disabled.

1: The generation of the overrun interrupt is enabled.

The ovres status generation should be disabled in case of access to data registers through multiple SPI accesses (not simultaneously with the burst mode). In this case, the interrupt is generated as soon as the second access is performed.

- **UNDES_EN: Underrun Interrupt Enable**

0: The generation of the underrun interrupt is disabled.

1: The generation of the underrun interrupt is enabled.

- **ADC_RDY_EN: ADC Ready Interrupt Enable**

0: The generation of the ADC ready interrupt is disabled.

1: The generation of the ADC ready interrupt is enabled.

7.41 Interrupt Status Register

Name: ITSR

Access: Read-only

7	6	5	4	3	2	1	0
–	–	–	–	–	ADC_RDY	UNDES	OVRES

- **OVRES: Overrun Status**

An overrun occurs when the host reads the data registers twice without updating the register values.

The ovres status generation should be disabled if data registers are read by multiple SPI accesses (not at once with the burst mode). In this case, the interrupt will be generated as soon as the second read access is performed.

This register is reset on read.

- **UNDES: Underrun Status**

An underrun occurs when two data register updates occur without read operation.

This register is reset on read.

- **ADC_RDY: ADC Ready Status**

ADC ready interrupt is generated as soon as one ADC conversion is performed.

This register is reset on read.

7.42 Software Reset Register

Name: SOFT_NRESET

Access: Write-only

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	NRESET

- **NRESET: Chip Reset**

When low, the entire chip is in reset state except the SPI interface and the SOFT_NRESET register.

When high, the reset state is released.

8. Software Example

This section details the steps to power up the ATSENSE-101/ATSENSE-201(H)/ATSENSE-301(H) devices.

1. Power the VDDIO / VDDIN plane with a 3.3V voltage.
2. If internal VDDA regulator is not used, power the VDDA pin with a 2.8V voltage.
3. If internal voltage reference is not used, power the VREF pin with a 1.2V standard voltage reference.
4. Release the internal reset:
   – SPI_WRITE 0x01 @ 0x2D [SOFT_NRESET].
5. If used, start the VDDA regulator:
   – SPI_WRITE 0x04 @ 0x27 [ANA_CTRL].
6. Start the analog BIAS generator:
   – SPI_WRITE 0x05 @ 0x27.
7. If used, start the voltage reference:
   – SPI_WRITE 0x07 @ 0x27. Wait 100 ms to account for VREF settling.
8. Enable the interrupts:
   – SPI_WRITE 0x07 @ 0x2A [ITCR],
9. Enable the output interrupt line:
   – SPI_WRITE 0x07 @ 0x2B [ITOUTCR],
10. Start the converters:
    – SPI_WRITE 0x31 @ 0x20 [SDI0], channel I0 ON with gain x8,
    – SPI_WRITE 0x31 @ 0x21 [SDI1], channel I1 ON with gain x8,
    – SPI_WRITE 0x01 @ 0x22 [SDV1], channel V1 ON,
    – SPI_WRITE 0x31 @ 0x23 [SDI2], channel I2 ON with gain x8,(2)
    – SPI_WRITE 0x01 @ 0x24 [SDV2], channel V2 ON,(1)
    – SPI_WRITE 0x31 @ 0x25 [SDI3], channel I3 ON with gain x8,(2)
    – SPI_WRITE 0x01 @ 0x26 [SDV3], channel V3 ON.(2)
11. Upon interrupt line ITOUT negative edge, read the ADC conversion results in registers ranging from address 0x00 to 0x1B.

Notes: 1. Only for ATSENSE-201(H)/ATSENSE-301(H).
2. Only for ATSENSE-301(H).

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

Table 9-1. Absolute Maximum Ratings*

Storage temperature	-55°C to +150°C
Power Supply Input on VDDIO, VDDIN	-0.3V to +4.0V
Digital I/O Input Voltage	-0.3V to +4.0V
Analog Input Voltage on VPx, VN, IPx, INx	-2.0V to +4.0V
All Other Pins	-0.3V to +4.0V
Maximum Output Current per Pin	100 mA
ESD (all pins)	2 KV HBM(1)

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

Notes: 1. According to specifications MIL-883-Method 3015.7 (HBM - Human Body Model)

9.2 Recommended Operating Conditions

Table 9-2. Recommended Operating Conditions

Parameter	Condition	Min	Max	Units
Operating Ambient Temperature	–	-40	85	°C
Power Supply Input	V_{VDDIO} ,V_{VDDIN}	3.0	3.6	V
Digital I/O Input Voltage	–	-0.3	V_{VDDIO} + 0.3	V
Analog Inputs Voltage Range	On $I_{P\{0,1,2,3\}}$, $I_{N\{0,1,2,3\}}$ and $V_{P\{1,2,3\}}$	-0.25	0.25	V

9.3 Current Consumption

Table 9-3. Current Consumption

Symbol	Parameter	Comments	Min	Typ	Max	Units
I_{DD_OFF}	Device not started.	Master Clock not running. V_{VDDIO} = V_{VDDIN} = 3.3V	–	1	2	µA
$I_{DD\_ON\_k.ADC}$	k Channels ON (k≥1), Voltage Reference ON, LDO regulator ON.	Master Clock @ 4.096 MHz, V_{VDDIO} = V_{VDDIN} = 3.3V	–	1.4 + k × 0.75	1.9 + k × 1.1	mA

9.4 Power-On-Reset Thresholds

Table 9-4. Power-On-Reset Thresholds

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{T_RISE}	V_{VDDIO} Rising Threshold	DC level	2.5	2.6	2.8	V
V_{T_FALL}	V_{VDDIO} Falling Threshold	DC level	2.35	2.5	2.65	V
V_{T_HYST}	V_{T_RISE} - V_{T_FALL}	–	90	120	180	mV

9.5 Digital I/Os DC Characteristics

Table 9-5. Digital I/Os Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{VDDIO}	Operating Supply Voltage	–	3.0	–	3.6	V
V_{IL}	Input Low-Level Voltage	–	-0.3	–	$0.3 \times V_{VDDIO}$	V
V_{IH}	Input High-Level Voltage	–	$0.7 \times V_{VDDIO}$	–	$V_{VDDIO} + 0.3$	V
V_{OL}	Output Low-Level Voltage	I_O max.	–	–	$0.25 \times V_{VDDIO}$	V
V_{OH}	Output Low-Level Voltage	I_O max.	$0.75 \times V_{VDDIO}$	–	–	V
I_O	Output Current (sink or source)	–	–	–	8	mA

9.6 Measurement Channels

Unless otherwise specified: External components according to Section 3. "Application Block Diagram": C_{VREF} = 1 µF and C_{VDDA} = 1 µF, MCLK = 4.096 MHz, V_{DDIN} = V_{DDIO} = 3.3V, Noise Bandwidth = [30Hz, 2kHz], T_J = [-40°C ; +100°C]

Table 9-6. Measurement Channel Electrical Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{VDDA}	Operating Supply Voltage	–	2.7	2.8	2.9	V
I_{VDD}	Channel Supply Current(1) in VDDIO and VDDA	OFF	–	–	1	µA
		ON	–	0.75	1	mA
f_{MCLK}	Master Clock Input Frequency	–	3.9	4.096	4.3	MHz
$Duty_{MCLK}$	Master Clock Input Duty Cycle	–	48	–	52	%
V_{IND_FS}	A/D Converter Input Referred Full Scale Voltage(2)	V_{REF} = 1.2V V_{IND} = V_{VPx} or V_{IND} = V_{IPx} - V_{INx} G: Channel Gain = {1, 2, 4 or 8}	–	1.2 / G	–	V_{PP}
V_{CM_IN}	Common Mode Input Voltage Range	(V_{IPx} + V_{INx}) / 2	-20	–	20	mV
Z_{IN0}	Common Mode Input Impedance at T_{J0} = 23°C	G: Channel Gain = {1, 2, 4 or 8} On V_{Px} , V_{IPx} , V_{INx} pins. F_{MCLK} = 4.096 MHz	400 / G	480 / G	560 / G	kΩ
$SINAD_{PEAK}$	Peak Signal to Noise and Distortion Ratio F_{IN} = 45 to 66Hz BW = [30 Hz, 2 kHz]	Gain = 1, V_{IND} = 1.000 V_{PP}	–	84	–	dB
		Gain = 1, V_{IND} = 0.500 V_{PP}(3)	–	78	–	
		Gain = 2, V_{IND} = 0.500 V_{PP}	–	84	–	
		Gain = 4, V_{IND} = 0.250 V_{PP}	–	82	–	
		Gain = 8, V_{IND} = 0.125 V_{PP}	–	81	–	
E_N	Input Referred Noise Voltage integrated over [30 Hz, 2 kHz]	Gain = 1	–	21	–	$µV_{RMS}$
		Gain = 2	–	10	–	
		Gain = 4	–	6	–	
		Gain = 8	–	3.3	–	
S_N	Input Referred Noise Voltage Density at fundamental frequency. (Between 45 and 66 Hz)	Gain = 1	–	470	–	nV/√Hz
		Gain = 2	–	220	–	
		Gain = 4	–	130	–	
		Gain = 8	–	73	–	
EG_0	Gain Error	T_{J0} = 23°C. V_{REF} = 1.2V	-3	–	3	%
TC_G	Channel Gain drift with temperature(4)	-40°C < T_J < 100°C, V_{REF} = 1.2V R_{SOURCE} = 3kΩ	–	-5	–	ppm /°C
V_{OS0}	Input Referred Offset	T_{J0} = 23°C	-5 / G	–	5 / G	mV
TC_{VOS}	V_{OS} drift with temperature	-40°C < T_J < 100°C	-2	–	+2	µV/°C

Notes:
1. Current consumption per measurement channel.
2. V_{IND} may be limited by the recommended input voltage on analog input pins (±0.25V, See Table 9-2, "Recommended Operating Conditions").
3. Corresponds to the maximum signal on the voltage channel(s).
4. Includes the input impedance drift with temperature.

9.7 Voltage Reference and Die Temperature Sensor

Unless otherwise specified: External components according to Section 3. "Application Block Diagram": C_{VREF}=1 µF and C_{VDDA} =1 µF, MCLK = 4.096 MHz, V_{VDDIN} = V_{VDDIO} = 3.3V, T_J = [-40°C; +100°C].

Table 9-7. Voltage Reference and Die Temperature Sensor Electrical Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{VDDA}	Operating Supply Voltage	–	2.7	2.8	2.9	V
I_{VDDA}	Supply Current	OFF	–	–	0.1	µA
		ON	–	70	100	
V_{REF0}	Output voltage initial accuracy	At T_{J0} = 23°C	1.142	1.144	1.146	V
TC_{VREF_U}	V_{REF} drift with temperature(1)	Uncompensated	–	50	–	ppm /°C
TC_{VREF_C}		Using factory programmed calibration registers.	–	10	–	
R_{OUT}	V_{REF} output resistance	–	200	500	800	Ω
D_{TEMP_Lin}	Die Temperature Sensor, Digital Reading Linearity	–	–	+/-2	–	°C
I_{VREF_OFF}	Current in VREF pin when internal voltage reference is OFF	–	-100	–	100	nA

Note: 1. TC is defined using the box method: TC = (V_{REF_MAX} - V_{REF_MIN}) / (V_{REF0} x (T_{MAX} - T_{MIN}))

9.8 VDDA LDO Regulator

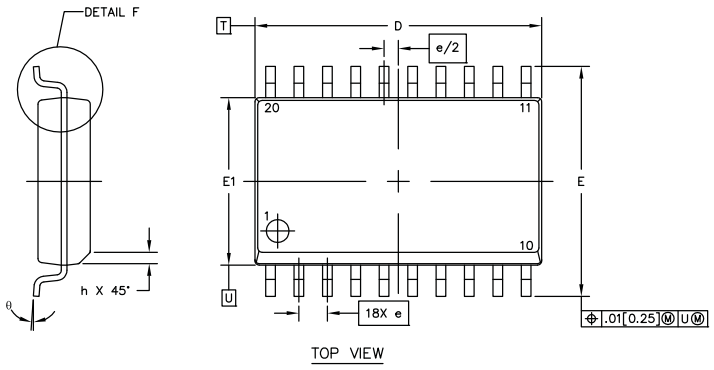
Unless otherwise specified: External components according to Section 3. "Application Block Diagram": C_{VREF} = 1 µF and C_{VDDA} = 1 µF, MCLK = 4.096 MHz, V_{DDIN} = V_{DDIO} = 3.3V, T_J = [-40°C; +100°C].

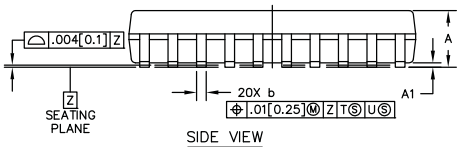
Table 9-8. VDDA LDO Regulator

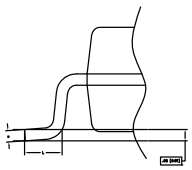
Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{VDDIN}	Operating Supply Voltage	–	3.0	3.3	3.6	V
I_{VDDIN}	Supply Current	OFF	–	–	0.1	µA
		ON	–	–	250	
I_O	Output Current	–	–	–	15	mA
V_O	DC Output Voltage	I_O = 0mA	2.75	2.8V	2.85	V
dV_O / dI_O	Static Load Regulation	I_O: 0 to I_{OMAX}	-5	–	–	mV/mA
dV_O/ dV_{VDDIN}	Static Line Regulation	V_{DDIN}: 3.0V to 3.6VV	-5	–	+5	mV/V
PSRR	Power Supply Rejection Ratio	f = DC to 2000 Hz	–	40	–	dB
		f = 1 MHz	–	40	–	
t_{START}	Start-Up time	V_O from 0 to 95% of final value. I_O= 0mA	–	–	1	ms
C_O	Stable Output Capacitor Range	Capacitive	0.5	1	4.7	µF
		Resistive	5	10	300	mΩ

10. Mechanical Characteristics

Figure 10-1. 20-lead SOIC Package





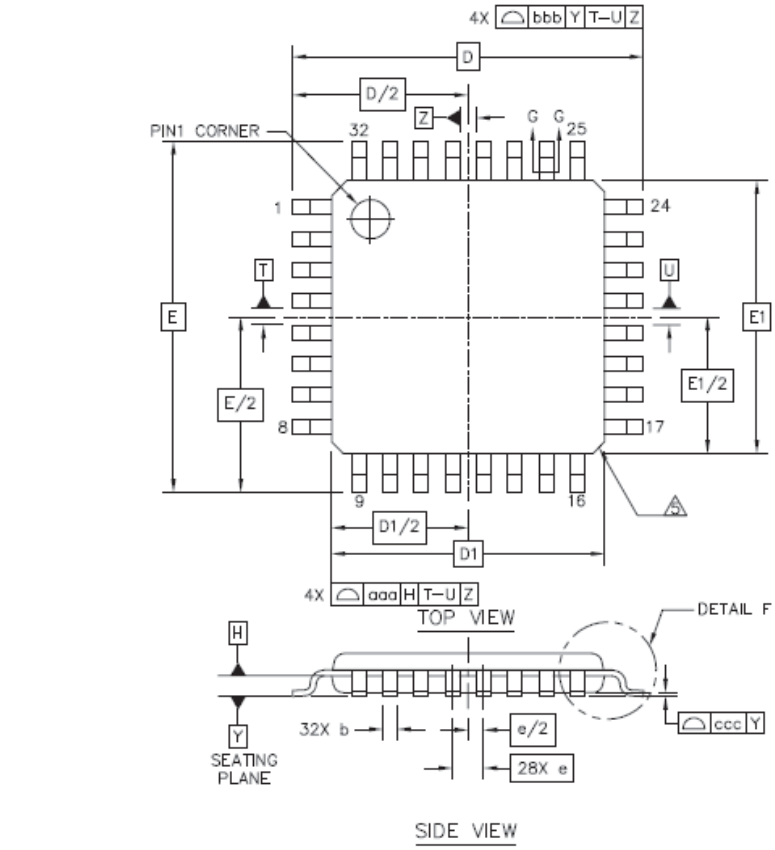


DETAIL F
ROTATED 90° CCW
SCALE: 20/1

	SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.093		.104	2.35		2.65
STAND OFF	A1	.004		.012	0.1		0.3
LEAD WIDTH	b	.013		.020	0.33		0.51
L/F THICKNESS	c	.009		.013	0.23		0.32
BODY SIZE	D	.496		.512	12.6		13
	E1	.291		.299	7.4		7.6
	E	.394		.419	10		10.65
LEAD PITCH	e	.050 BSC			1.27 BSC		
	L	.016		.050	0.4		1.27
	h	.010		.030	0.25		0.75
	θ	0°		8°	0°		8°

	TITLE	Small Outline Package - 300 MIL			GPC:	S R J
Atmel	Pins:	20		Drawing No.:	R-SO020_H	
	Body:	12.8x7.5x2.3	mm	REV.:	A	
	Lead Pitch :	1.27	mm	Date:	2/26/2013	
			mm	Jedec Code:	MS-013-C	

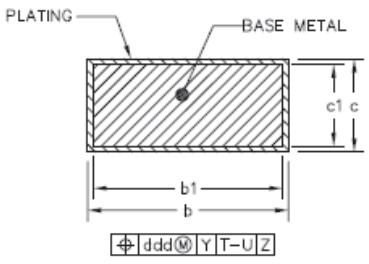
Figure 10-2. 32-lead TQFP Package



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.2
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	0.95	---	1.05
LEAD WIDTH(PLATING)		b	0.32	0.37	0.42
LEAD WIDTH		b1	0.32	0.35	0.38
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.8 BSC		
		L	0.5	0.6	0.7
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.1		
LEAD OFFSET		ddd	0.2		
MOLD FLATNESS		eee	0.05		

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.



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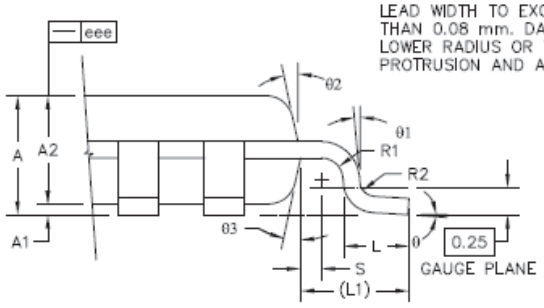

DETAIL F
SCALE: 20/1

Sept 20, 2012.

	TITLE	GPC	DRAWING NO.	REV.
Atmel	Thin Quad Flat Pack (TQFP), 32 Pins Body: 7 x 7 x 1.0 mm Pitch 0.8 mm	AUT	R-TQ032_E	A

11. Ordering Information

Table 11-1. Ordering Information

Ordering Code	Package	Carrier Type	Package Type	Temperature Operating Range
ATSENSE101A-SUR	SOIC20	Tape & Reel	Green	Industrial (-40°C to +85°C)
ATSENSE101A-SU	SOIC20	Tube		
ATSENSE201A-AUR	TQFP32	Tape & Reel		
ATSENSE201HA-AUR				
ATSENSE201A-AU	TQFP32	Tray		
ATSENSE201HA-AU				
ATSENSE301A-AUR	TQFP32	Tape & Reel		
ATSENSE301HA-AUR				
ATSENSE301A-AU	TQFP32	Tray		
ATSENSE301HA-AU				

12. Revision History

In the table that follows, the most recent version of the document appears first.

Table 12-1. ATSENSE-101/-201(H)/-301(H) Datasheet Rev. 11219B Revision History

Doc. Date	Changes
20-Feb-14	Removed preliminary status.
	ATSENSE-201(H) device added to the datasheet in "Description" and"Features".
	Figure 3-2 "ATSENSE-201(H) Typical Application Block Diagram" added.
	Section 2. "Package and Pinout": added ATSENSE-201(H)
	Updated register descriptions for use with ATSENSE-201(H) from "ADCI2 TAG Register" to "ADCV3 Output Bits 7 to 0 Read Register" and from "ADCI2 Controls Register" to "ADCV3 Controls Register".
	Section 9.6 "Measurement Channels", Section 9.7 "Voltage Reference and Die Temperature Sensor" and Section 9.8 "VDDA LDO Regulator": In introduction text, corrected $C_{VREF}$and C_{VDDA} units to µF.
	Table 9-6 "Measurement Channel Electrical Characteristics": Added condition with typ value for $SINAD_{PEAK}$
	Table 9-8 "VDDA LDO Regulator": Updated min, typ and max values and modified units for parameters Static Load Regulation and Static Line Regulation. Changed typ value for parameter Power Supply Rejection Ration for condition f = 1 MHz.
	Table 11-1 "Ordering Information": added ATSENSE-201(H) ordering codes. Added ATSENSE101A-SUR.

Table 12-2. ATSENSE-101/-301(H) Datasheet Rev. 11219A 15-Oct-13 Revision History

Doc. Date	Changes
15-Oct-13	First Issue

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